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INFORMATION PLOOP COURS	Application Number		
INFORMATION DISCLOSURE	Filing Date	15 August 2003	
STATEMENT BY APPLICANT	First Named Inventor	Chih C. YEH et al.	
	Group Art Unit		
(use as many sheets as necessary)	Examiner Name		

Attorney Docket Number

				U.S. PATENT DOC	JMENTS	
Examiner Initials'	Cite No.1	Number (ii	ument nd Code ² known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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		Office ³	Number ⁴	Kind Code ^s (<i>if known</i>)	Applicant of Cited Document	Cited Document MM-DD-YYYY	Where Relevant Passages or Relevant Figures Appear	Te
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^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁹ Applicant is to place a check mark here if English language Translation is attached.

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	INFORMATION DISCLOSURE			Application Number	
INF			CLOSURE	Filing Date	15 August 2003
STA	STATEMENT BY APPLICANT			First Named Inventor	Chih C. YEH et al.
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	(use as many sheets as necessary)			Examiner Name	
Sheet	2	of	2	Attorney Docket Number	MXIC 1553-3

		OTHER PRIOR ART NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (In CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
ØNI	C1	C. de GRAAF et al., "A Novel High-Density Low-Cost Diode Programmable Read Only Memory" Philips Research Labs., Prof. Holstlaan 4, 5656AA Eindhoven, The Netherlands, 1996 IEDM, pps. 189-192.	
	C2	M. JELINEK et al., "Hybrid PLD Technique for Nitrogen Rich CNx Layers", Lasers and Electro-Optics Europe, 2000. Conf. Digest. 2000 Conf. on, 10-15 Sept 2000, 1 page.	
	C3	B. LINDER et al., "Growth and Scaling of Oxide Conduction After Breakdown", 41st Annual Int'l Reliability Physics Symposium, Dallas, TX, 2003, pp. 402-405.	
	C4	S. ROSSNAGEL et al., "From PVD to CVD to ALD for Interconnects and Related Applications", Interconnect Technology Conf., 2001. Proceedings of the IEEE 2001 Int'l, 4-6 June 2001, pp. 3-5.	
240	C5	X.W WANG et al., "Ultra-Thin Silicon Nitride Films on Si by Jet Vapor Deposition", VLSI Technology, Systems and Applications, 1995, Proceedings of Technical Papers, 1995 International Symposium on, 31 May-2 June 1995, pp. 49-52.	
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Sheet

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Col	Complete if Known			
Application Number	10/642,249			
Filing Date	15 August 2003			
First Named Inventor	Chih C. Yeh et al.			
Art Unit	Unassigned			
Examiner Name	Unassigned			
Attorney Docket Number	MXIC 1553-3			

Examiner	Cite	Document Number	Publication Date	DOCUMENTS Name of Patentee or	Pages, Columns, Lines, Where
Initials*	No.1	Number-Kind Code ^{2 (F Incom)}	MM-DD-YYYY	Applicant of Cited Document	Relevant Passages or Relevant Figures Appear
WW.	A1	^{US-} 5,012,448	04-30-1991	Matsuoka et al.	
	A2	^{US-} 5,457,650	10-10-1995	Sugiura et al.	
	А3	^{US-} 5,543,738	08-06-1996	Lee et al.	
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1 6	A6	^{US-} 5,721,701	02-24-1998	lkebe et al.	
RN19	A7	^{US-} 5,729,490	03-17-1998	Calligaro et al.	
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		FOREI	GN PATENT DOCU	MENTS		
Examiner Cite	Cite No.1	Foreign Patent Document	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages	Γ
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		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
DVO	C1	Takuji Hosoi et al. "A New Model of Time Evolution of Gate Leakage Current After Soft Breakdown in Ultra-Thin Gate Oxides" IEEE February 2002 pages 155-158.	
Ok0	C2	Tahui Wang et al. "Negative Substrate Bias Enhanced Breakdown Hardness in Ultra-Thin Oxide pMOSFETs" IEEE 41st Annual International Reliability Physics Symposium, Dallas, Texas August 2003 pages 437-441.	

Examiner Signature	Dask W. One	Date Considered	18/05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known				
Application Number	10/642,249			
Filing Date	15 August 2003			
First Named Inventor	Chih C. Yeh et al.			
Art Unit	2818			
Examiner Name	Unassigned			
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	U. S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ^{2 (f known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1

Complete if Known **Application Number** 10/642,249 Filing Date 15 August 2003 First Named Inventor Chih C. Yeh et al. Art Unit 2818 **Examiner Name** Unassigned MXIC 1553-3 Attorney Docket Number

Examiner Initials*	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant	
	<u> </u>	Number-Kind Code ^{2 (F known)}			Figures Appear	
	A1	^{US-} 5,093,711 A1	03-03-1992	Kazuki Hirakawa	,	
7	A2	^{US-} 5,350,710 A	09-27-1994	Hong et al.		
	A3	^{US-} 6,432,782 B1	08-13-2002	Lung et al.		
	A4	^{US-} 6,534,841 B1	03-18-2003	Van Brocklin et al.		
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	A8	^{US-} 6,618,295 B2	09-09-2003	Scheuerlein		
	A9	^{US-} 6,677,220 B2	01-13-2004	Van Brocklin et al.		
	A10	^{US-} 6,703,652 B2	03-09-2004	Van Brocklin et al.		
	A11	^{US-} 6,704,235 B2	03-09-2004	Knall et al.		
	A12	^{US-} 2003/0080370 A1	05-01-2003	Harari et al.	,	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known			
Application Number	10/642,249		
Filing Date	15 August 2003	_	
First Named Inventor	Chih C. Yeh et al.		
Art Unit	2818		
Examiner Name	Unassigned		
Attorney Docket Number	MXIC 1553-3		

			U. S. PATEN	DOCUMENTS	
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ² (# known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
(NO)	A1	^{US-} 6,650,143	11-18-2003	Peng	
	A2	^{US-} 6,667,902	12-23-2003	Peng	
	A3	us- 6,671,040	12-30-2003	Fong et al.	
	A4	US- 6,700,151	03-02-2004	Peng	
	A5	US- 2002/0094611	07-17-2002	Wu et al.	•
	A6	US- 2004/0008538	01-15-2004	Peng	
	A7	US- 2004/0047218	03-11-2004	Peng	
	A8	US- 2004/0106251	06-03-2004	Forbes et al.	
+0/0	A9	US-2004/0129995	07-08-2004	Yeo et al.	
ENG	A10	US- 2004/0137688	07-15-2004	Chang et al.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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of 2

	Complete if Known	
Application Number	10/642,249	
Filing Date	15 August 2003	
First Named Inventor	Chih C. Yeh et al.	
Art Unit	2818	-
Examiner Name	Unassigned	
Attorney Docket Number	MXIC 1553-3	

	-	NON PATENT LITERATURE DOCUMENTS	
Examine Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
DKG) C1	Stathis, J.H., "Reliability Limits for the Gate Insulator in CMOS Technology" IBM. J. Res. & Dev., Vol. 46, No. 2/3, March/May 2002, 265-286	
	C2	Miranda, Enrique, et al. "Analytic Modeling of Leakage Current Through Multiple Breakdown Paths in SiO2 Films" IEEE 39th Annual IRPS 2001, 367-379	
	C3	Wu, E.Y. et al., "Voltage-Dependent Voltage-Acceleration of Oxide Breakdown for Ultra- Thin Oxides" Electron Devices Meeting, 2000, IEDM Technical Digest International, 10- 13 December 2000, 541-544	
	C4	Sune, Jordi et al. "Post Soft Breakdown Conduction in SiO2 Gate Oxides" Electron Devices Meeting, 2000 IEDM Technical Digest International, 10-13 Dec. 2000 533-536	
	C5	Rasras, Mahmoud et al. "Substrate Hole Current Origin After Oxide Breakdown" Electron Devices Meeting, 2000 IEDM Technical Digest International, 10-13 Dec. 2000, 537-540	
	C6	Lombardo, S., et al. "Softening of Breakdown in Ultra-Thin Gate Oxide nMOSFETs at Low Inversion Layer Density" Reliability Physics Symposium 2001, Proceedings 39th Annual 2001 IEEE International, 30 April, 3 May 2001, 163-167	
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Examiner Date Considered 1/18/05
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
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